programmable sequencer

Sequencers are extremely popular add-on units for music synthesisers. They are used to store pre-programmed sequences of control voltages for the synthesiser VCOs/VCFs; the control voltages can be 'played back' into the synthesiser, thereby generating note sequences which can be used for example to provide the backing to a manually played melody.

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There are a variety of different ways in which the control voltages can be programmed and stored: e.g. via potentiometers, switches, sample-and-hold circuits or digital memories. The method adopted here is to encode the voltage digitally and store it in a RAM. When the contents of the memory are read out, they are fed to a D/A converter, which provides an analogue signal suitable for feeding to the synthesiser VCOs. In addition to the pitch of the notes (i.e. their frequency), their relative length can also be programmed. The duration of each note can be selected in the ratio of 1 : 2 : 4 : 8. The block diagram of the programmable circuit and the 'subsidiary' address counter, however, even longer (or indeed shorter) sequences are also possible. The note length is controlled by a D/A converter and VCO, the output of which varies the clock frequency of the main address counter. The analogue voltages from output A are fed to the synthesiser VCOs; at output B a gate pulse is generated to accompany each note. The gate pulse, whose width can be varied, is used to determine the start and duration of the envelope control voltage generated by the ADSR module of the synthesiser. The complete circuit diagram of the programmable sequencer is shown in

sequencer is shown in figure 1. The pitch (i.e. its position on the musical scale and its octave) and length of the note are set up in binary code on switches which are connected to the data inputs of the RAM (see figure 3). The address into which the data is stored is determined by an address counter. In actual fact, two address counters are employed, one of which (the 'subsidiary' counter) is clocked by the other ('main' counter). When the stored melody is to be played back, the address counter steps through each of the memory locations in turn. The data is read out and fed to the digital-analogue converters, which provide the actual control voltages for the VCOs. During normal operation the circuit can store 16 sequences of 16 notes apiece, i.e. a combined sequence of 256 notes; with the aid of the reset figures 2a and 2b. Figure 2a contains the digital section of the sequencer, comprising the memory, address counter and reset circuit, whilst figure 2t[redacted]ows the D/A converters and output stages. Two 2101's, 256 x 4-bit RAMs, connected in parallel from the memory in which the digitally encoded control voltages are stored. The higher order addresses of the input data are set up on switches S2 . . . S5. The flip-flop (IC11) interposed between the switches and the RAMs ensure that the new address set up on S2 . . . S5 is only presented to the address inputs of the RAMs after the previous note sequence has ended.

The main address counter is formed by IC10. The counter is clocked, via IC6, by the analogue section of the circuit shown in figure 2b. This counter generates the 'low order' addresses,

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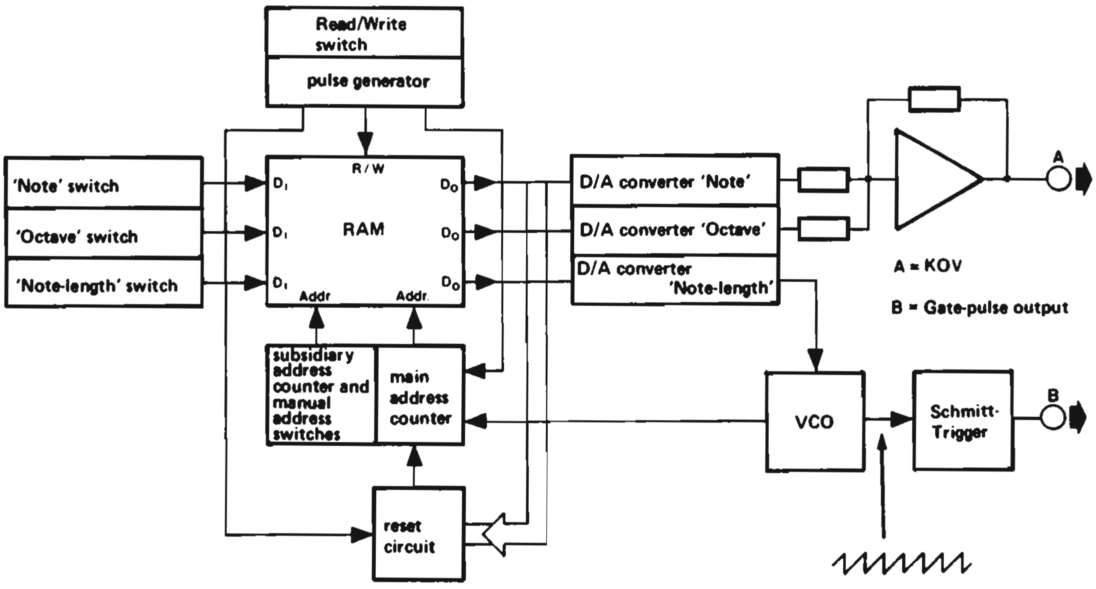
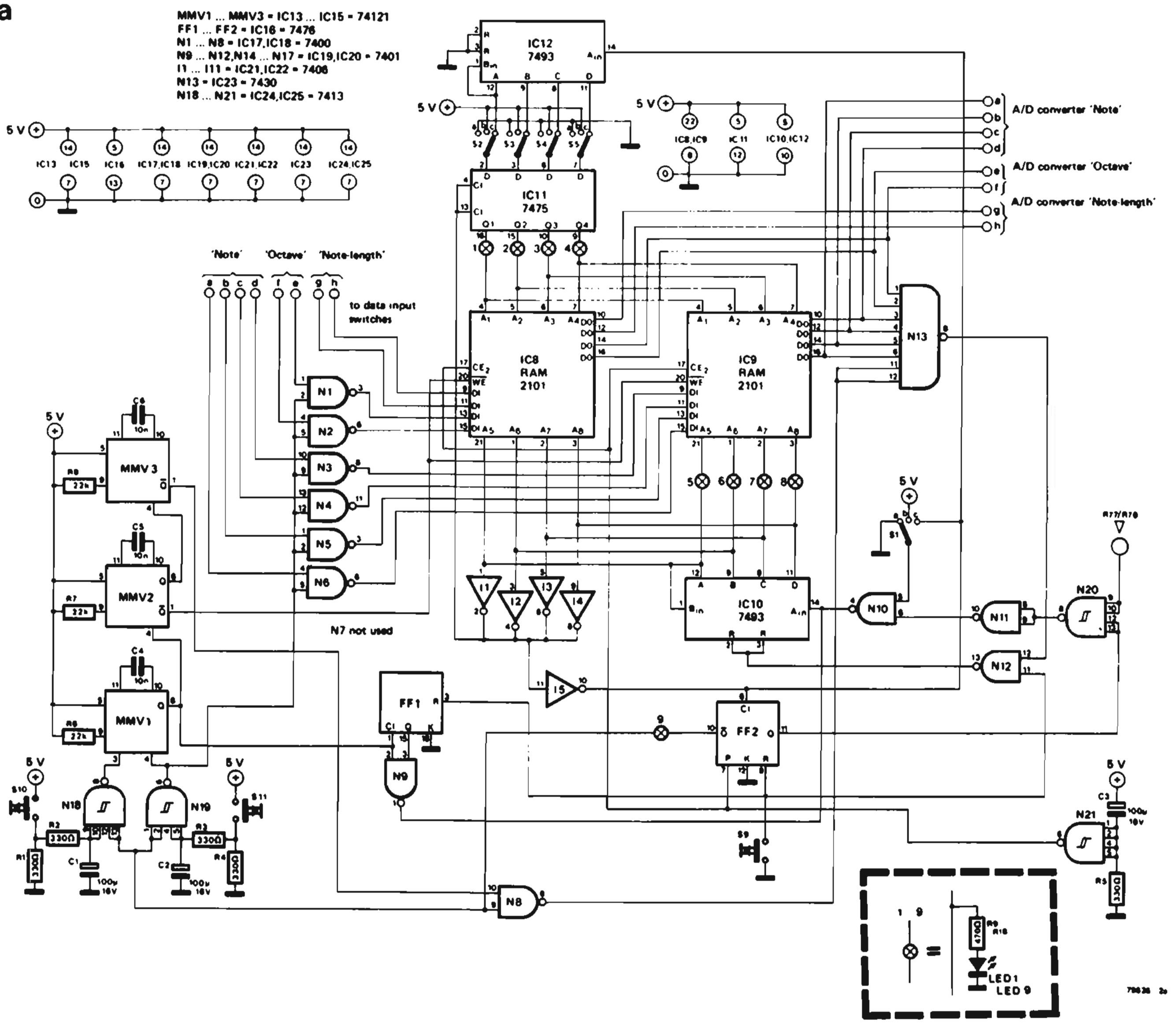


2a



i.e. it clocks from '0000' to '1111', whereupon the high order address is incremented by one (via S2 . . . S5), before the counter resets and starts to cycle through another sequence of 16 addresses.

The reset circuit is formed by N12 and N13. When the data outputs a . . . f of the RAM all go high, N12 and N13 ensure that the binary counter is reset to zero. Thus the address containing the data word '111111' represents the reset address. Inverters I1 . . . I4 form a NOR gate (the inverters all have open-collector outputs), so that only when the address counter resets (i.e. its outputs all go low), is IC11 clocked. This ensures that a new (high order) address cannot be presented to the address inputs of the RAMs before the previous note sequence has ended.

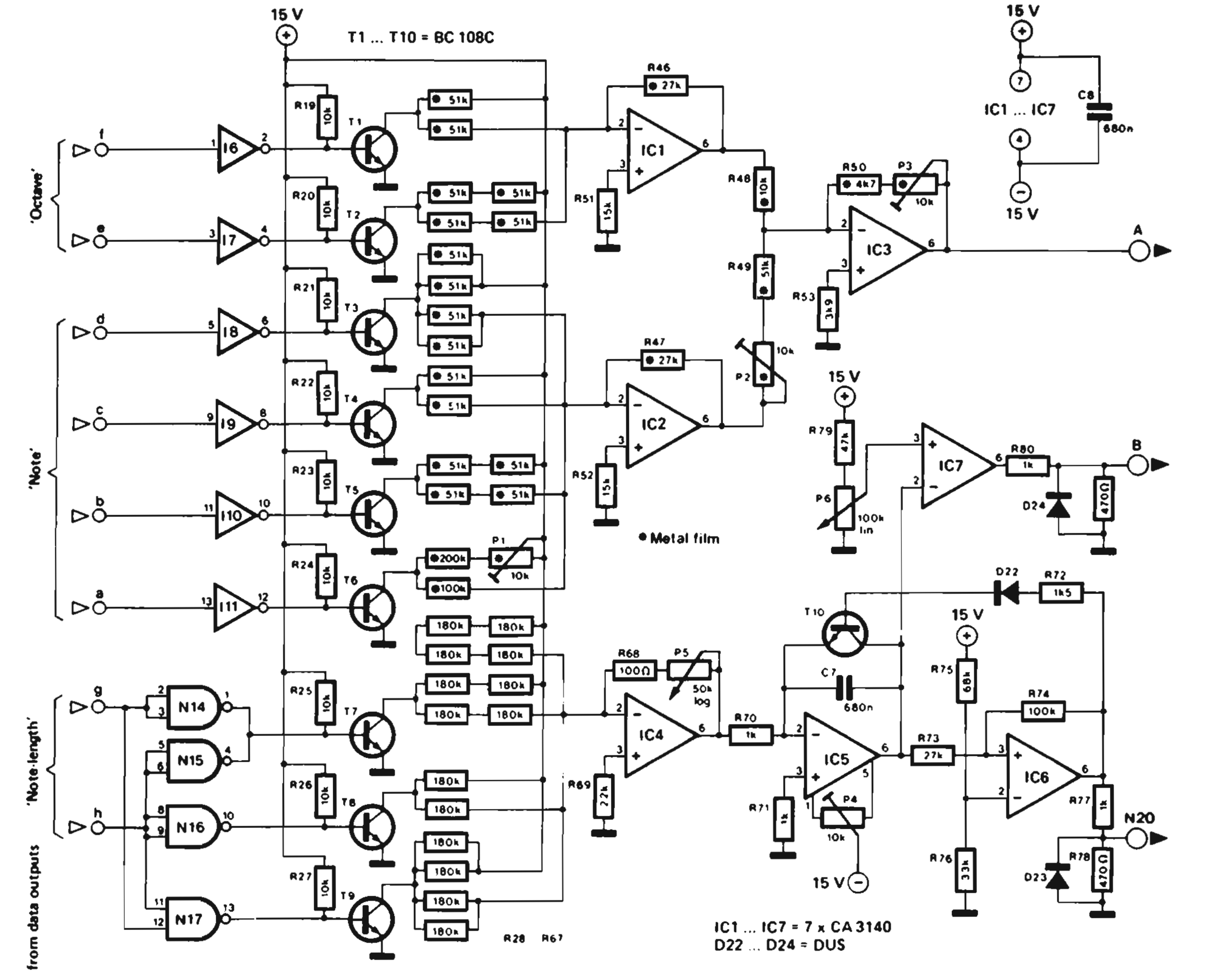
When S2 . . . S5 are set to position c, the 'subsidiary' address counter (IC12) is connected to the address inputs of the RAMs. This counter is clocked by IC10, via I1 . . . I5, so that it receives a clock pulse every time IC10 resets (i.e. every 16 addresses). Thus if all the outputs of IC12 are connected to the RAMs, the entire contents of the memory can be read out in sequence. Switch S1 determines the operating mode of the sequencer. In position a the switch blocks gate N10, with the result that the address counter is immediately inhibited. In position b the sequencer operates normally, whilst in position c the counter will stop once it reaches '0000'.

To actually program a sequence of notes into memory, pushbutton switch S9 is first pressed, resetting the address counter via N12 and enabling the RAMs. The information relating to the pitch and length of the note to be stored is then written into the RAMs by pressing S10. Each of the monostable multivibrators MMV1 . . . MMV3 are now triggered in turn. The output pulse from MMV1 clocks the address counter (IC10) via N9. The pulse from MMV2 temporarily puts the RAMs into the write mode, so that the information present on the data inputs is in fact stored in memory. The $\bar{Q}$ output of MMV3 takes the output of N8 high, so that N13 is capable of recognising the reset code ('111111') on the data outputs of the RAMs.

The next note is written into memory in the same way; the input data is set up on the corresponding switches whereupon S10 is pressed and the data is written into memory. Once the desired sequence of notes is stored, pressing S11 writes the reset code into the memory by taking the inputs of N1 . . . N6 low and hence the data inputs of the RAMs high. When N13 recognises the reset code, the address counter (IC10) is reset, so that via I1 . . . I5, flip-flop FF2 is triggered and the RAMs are returned to the read mode. Schmitt trigger N21 ensures that FF2 assumes a definite state upon switch-on and that the RAMs are inhibited for a brief initial period.

The digital-analogue converters and output stages of the circuit are shown in figure 2b. IC1 . . . IC3 produce the analogue control voltages which determine the frequency of the notes, whilst the D/A converter round IC4 is used to control the length of the notes. Unlike the other two D/A converters (IC1/IC2), the output voltage increases in an exponential, not linear fashion.

2b



That is to say, when the digital input signal increments by '01', the output voltage doubles.
The output of IC4 is fed to a sawtooth generator formed by IC4 and IC5; this both clocks the main address counter (IC10 in fig. 2a) and, via the Schmitt trigger IC7, provides a variable-width gate pulse.
In spite of the six adjustment points (potentiometers P1 . . . P6), the circuit can be set up fairly simply, without the need for any special measuring equipment. The circuit is adjusted correctly when a change in the 'e' input from '0' to '1' causes the voltage at output A to increase by 1 V. This voltage can be adjusted by means of P3. P2 should be set such that the output voltage changes by 0.5 V when inputs 'b' and 'c' go high.
Fine tuning is performed by means of P1. A change in state of input 'a' should correspond to a change of 1/12 V in the output signal. P5 should be adjusted such that the output frequency doubles when input 'g' goes high. P4 is used to compensate the offset voltages of IC4 and IC5. Finally, P6 determines the width of the gate pulse.

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