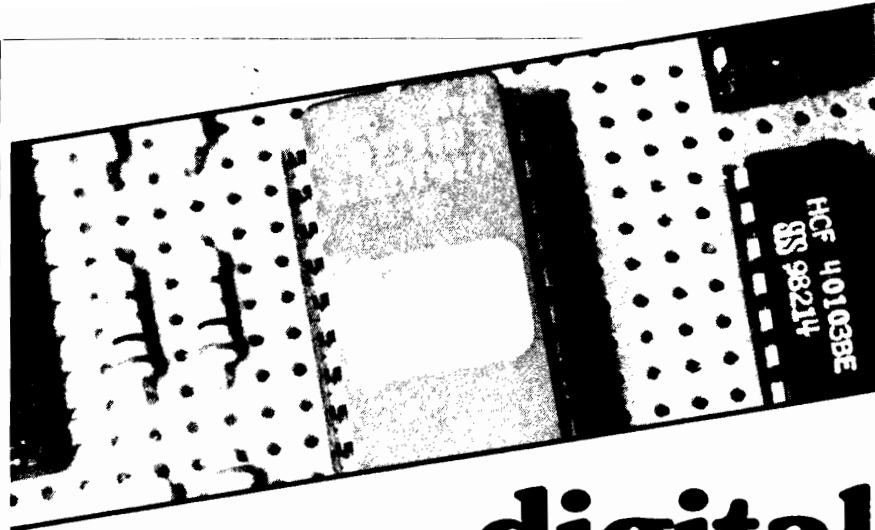


enthusiasts  
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The duty factor of a digital (pulse) signal is the ratio of the pulse width to the pulse spacing. It is sometimes, quite wrongly, called the duty cycle.

- tone = a musical sound consisting of a pure note (UK)  
= single sound of a given pitch and duration (USA)
- note = single sound of a given pitch and duration (UK)  
= a musical sound consisting of a pure note (USA)



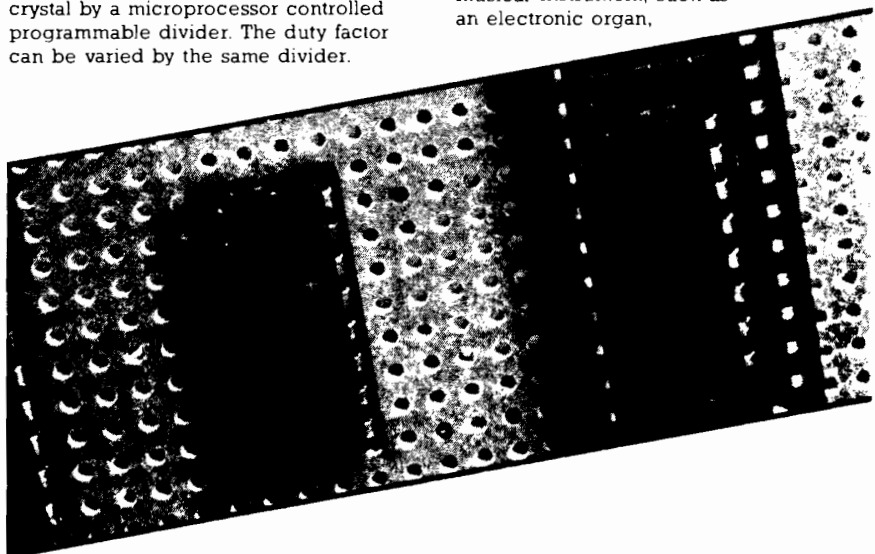
# digital oscillators

One of the real problems in electronic organs, synthesizers, and other polyphonic instruments is the stability of the oscillators, and the more oscillators there are, the more important tight tolerances become. Every hobbyist who has ever worked on a circuit containing a number of oscillators will know what we mean. One of the methods used to solve (or avoid) this problem is the use of digital techniques and a crystal to determine the frequency. Unfortunately, this procedure brings with it a fixed phase relation between separate signals, which detracts from the naturalness of the sounds. As we were not satisfied with this, we designed three circuits that may be used to replace the voltage-controlled oscillator (VCO) in an existing design, or that may form the basis of a new design.

In this article, a digitally controlled oscillator, DCO, is a circuit that generates rectangular signals with fixed or variable duty factor, the frequency of which is determined by a quartz crystal. The value of that frequency is related to that of the crystal by a microprocessor controlled programmable divider. The duty factor can be varied by the same divider.

## A first approach

Designing a DCO is no simple matter, not only in view of the theory involved, but also because of the sheer number of channels needed in a polyphonic musical instrument, such as an electronic organ,



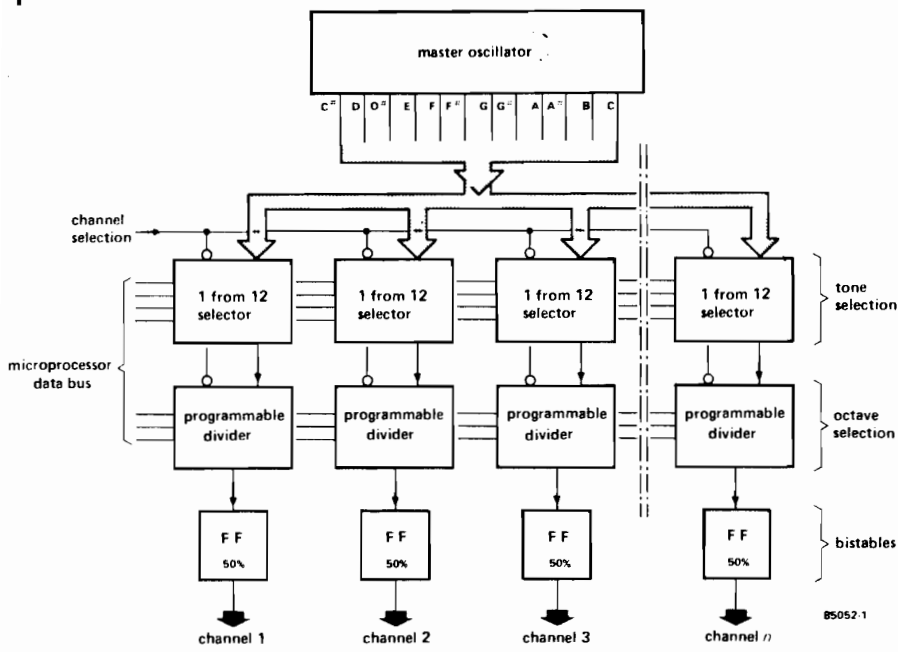


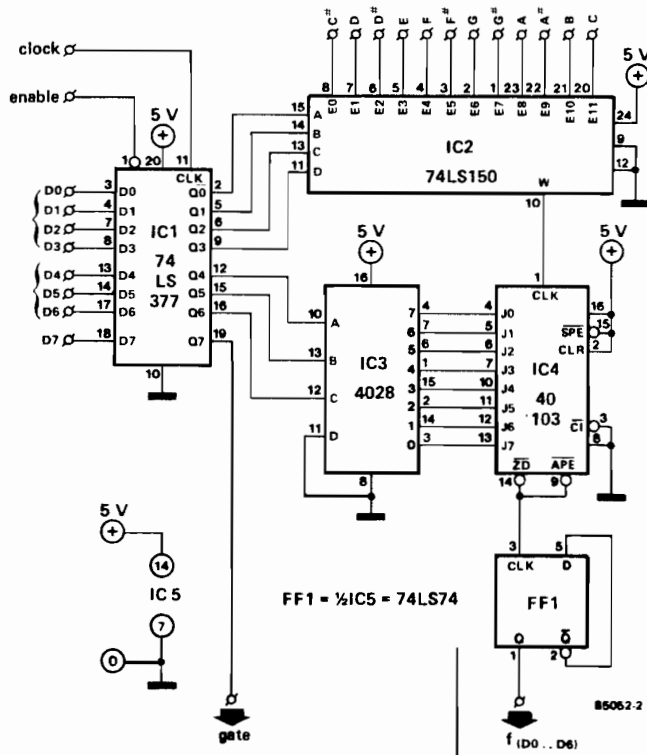
Figure 1. Block schematic diagram of a digital oscillator that may be the basis for a polyphonic musical instrument.

synthesizer, or piano. A single DCO is hardly ever encountered. The schematic diagram of a possible DCO is shown in figure 1. The master oscillator generates the twelve tones of an octave from which one is selected. The frequency of that tone is divided by 1, 2, 3...n to determine the octave number above or below middle C (261.63 Hz). The duty factor of the resulting signal is fixed at 50 per cent by a bistable, after which the signal is fed to one of n channels. Selection of the wanted tone, octave, and channel is effected by a microprocessor. The detailed circuit of one channel is given in figure 2: this must, of course, be duplicated as many times as there are channels required. The 74LS150 is used as a 1 from 12 decoder controlled by data lines D<sub>0</sub>...D<sub>3</sub>. The binary input to these lines determines which of the 12 frequencies applied to inputs E<sub>0</sub>...E<sub>11</sub> will be fed to pin 10. This output signal is taken to synchronous down-counter IC<sub>4</sub>, which is used here as a programmable divider. The divisor is determined by the information present on the microprocessor's D<sub>4</sub>...D<sub>6</sub> data lines. This information is first converted to a digital value by IC<sub>3</sub> and results in at least one of outputs 0...7 being active at any one time. This produces preset values, and divisors, of: 1, 2, 4, 8, 16, 32, 64, and 128. Lines D<sub>4</sub>...D<sub>6</sub> enable the required octave to be selected. To clarify all this, figure 3 shows some down-count cycles. The longer the down-count takes after APE has become active to reach zero (ZD active), the lower the frequency at the input. The bistable provides a train of very short negative pulses which have a duty factor of 50 per cent (i.e., they are square waves).

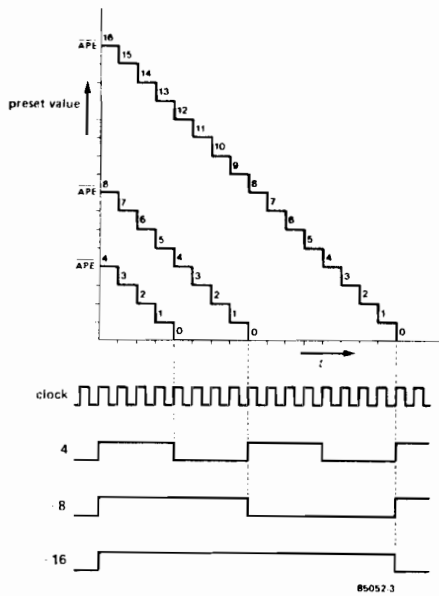
The circuit of figure 2 does not generate any signal, but is, rather, a sort of programmable interface between the microprocessor and the master oscillator. The master oscillator, the circuit of which is shown in figure 4, has buffered outputs which can, therefore, be applied to one or more 1 from 12 decoders (figure 2). The set-up of figure 5 is quite different from

Figure 2. Each channel in figure 1 requires a circuit as shown here. The tone and the octave are selected via the data bus.

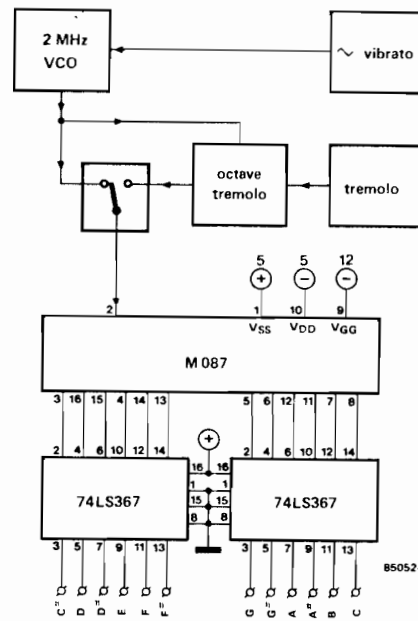
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Figure 3. The principle of the 40103 divider. The higher the preset value, the longer the counting process, and the lower the frequency.

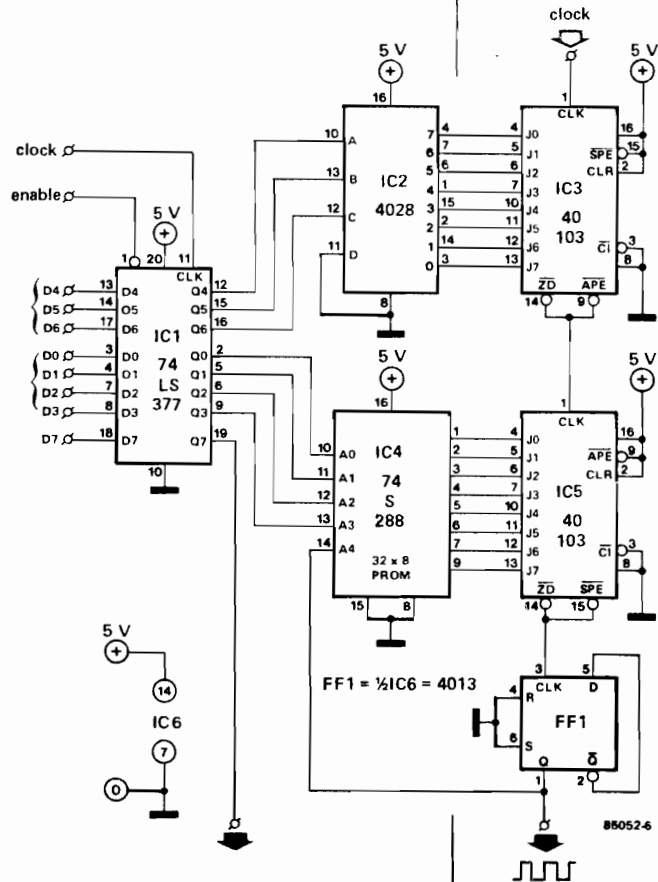
Figure 4. The M087 is a master oscillator that generates the twelve tones of an octave. It may be driven by a crystal oscillator, as here, or by a voltage-controlled oscillator, possibly in conjunction with a vibrato and tremolo circuit.

Figure 5. An alternative for one channel from figure 1. Two programmable dividers ensure selection of tones and octaves.

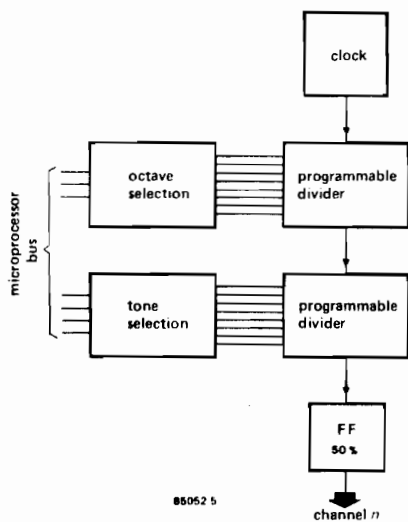
Figure 6. The circuit diagram of the set-up in figure 5. The clock frequency is equal to the highest tone of the highest octave.

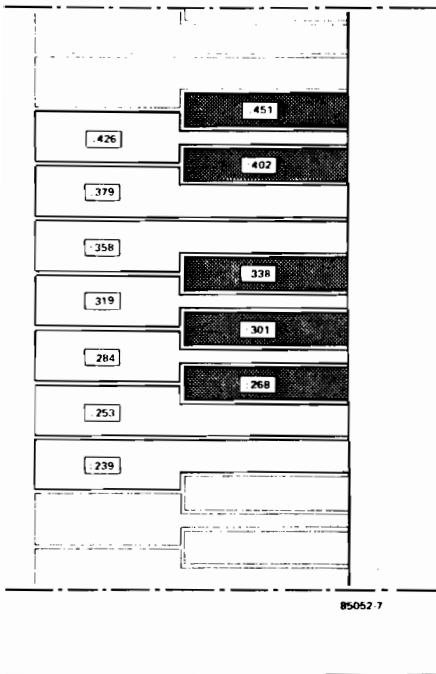
that in figure 1: it has no master oscillator, but simply a clock input, the frequency of which is a multiple of the highest tone in the top octave. This frequency is applied to two programmable dividers that select the octave and tone respectively. The circuit of this arrangement is shown in figure 6. The octave is selected by the microprocessor via retriggerable buffer IC<sub>1</sub>, and then applied to a divider formed by IC<sub>2</sub> and IC<sub>3</sub>. The frequency of the output of IC<sub>3</sub> is a multiple of the tone which will be selected by programmable divider IC<sub>5</sub>.

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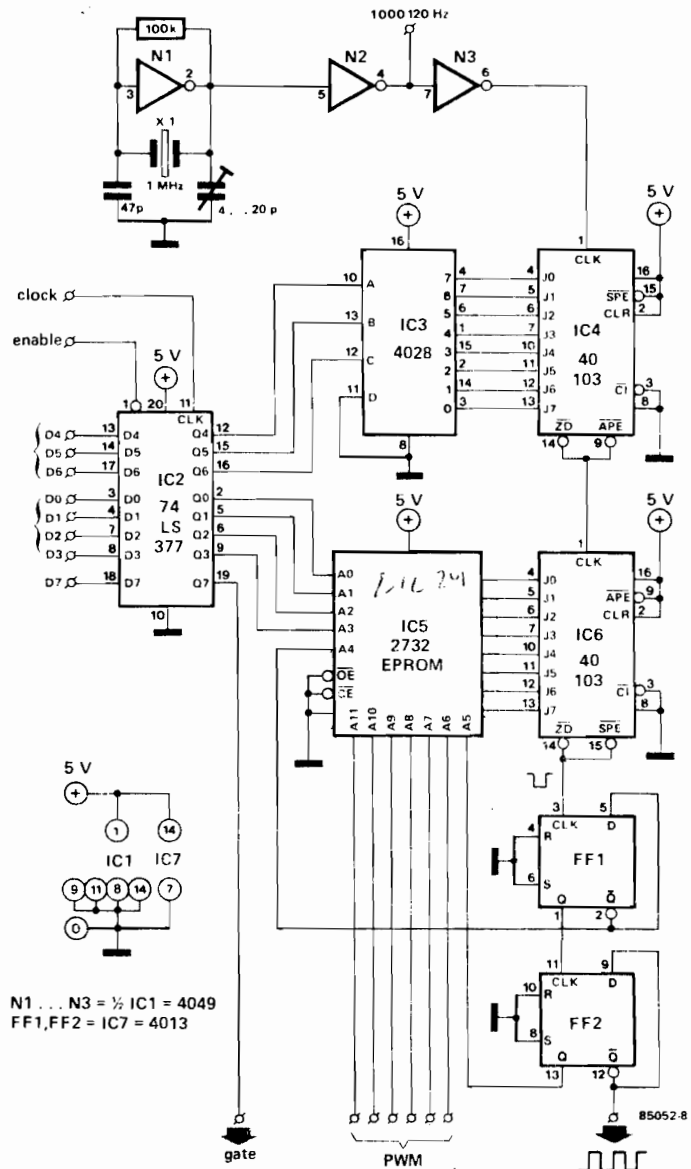
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The ratio between successive tones in an octave is the 12th power root of 2, which is very nearly equal to 1.059. These ratios are provided as a matter of course in an IC like the M087, but they can also be obtained from the set-up in figure 6, consisting of divider IC<sub>5</sub>, PROM IC<sub>4</sub>, and bistable FF<sub>1</sub>.

The divisors required to resolve an octave into its constituent twelve tones are shown in figure 7. The 40103 on its own can cope neither with numbers larger than 256, nor with odd numbers, but, in conjunction with a PROM, IC<sub>4</sub>, and the bistable, it can. The basic divide information is selected via D<sub>0</sub>...D<sub>3</sub>, which are connected to address lines A<sub>0</sub>...A<sub>3</sub> of the PROM via IC<sub>1</sub>. By feeding back output Q of the bistable to input A<sub>4</sub> of the PROM, it becomes possible to split the divide process into two. During one part of the count cycle the output of the bistable is logic low, when the lowest sixteen addresses of the PROM are selected. A certain preset value for IC<sub>5</sub> then exists at the memory location selected by D<sub>0</sub>...D<sub>3</sub>. After this value has been counted, the bistable toggles, and the highest sixteen addresses of the PROM are selected. Lines A<sub>0</sub>...A<sub>3</sub> do not change, so that the preset value is then sixteen places higher than previously. After this preset value has been counted, the bistable toggles again, and the whole process starts afresh. The contents of the PROM are given in table 1. Note a small but important point here: because the SPE input is now used as the preset enable instead of the  $\overline{APE}$  input, the divisor is the preset value plus 1. Therefore, the data values in table 1 are one lower than the wanted divisors.



N1...N3 = 1/2 IC1 = 4049  
FF1, FF2 = IC7 = 4013

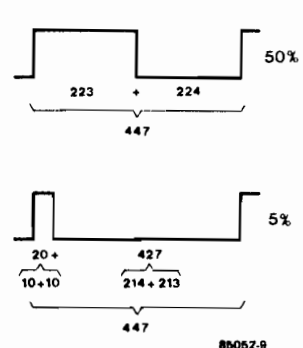


Figure 7. The divisors for resolving an octave into its twelve constituent tones.

Figure 8. This extended DCO provides twelve tones over eight octaves. The duty factor may be set between five and 50 per cent in sixty-four steps.

Figure 9. To achieve a variable duty factor, it is necessary to divide both count cycles once more: there are thus four count cycles per period.

Table 1.

A4	A3	A2	A1	A0	DATA HEX
0	0	0	0	0	F0
0	0	0	0	1	D4
0	0	0	0	1	C8
0	0	0	1	0	BC
0	0	0	1	1	B0
0	0	1	0	0	B2
0	0	1	0	1	A8
0	0	1	1	0	9E
0	0	1	1	1	90
0	1	0	0	0	8D
0	1	0	0	1	85
0	1	0	1	0	7D
0	1	0	1	1	76
1	0	0	0	0	E1
1	0	0	0	1	14
1	0	0	1	0	C8
1	0	0	1	1	BD
1	0	1	0	0	E2
1	0	1	0	1	9F
1	0	1	1	0	96
1	0	1	1	1	8D
1	1	0	0	0	85
1	1	0	0	1	7E
1	1	0	1	0	77
1	1	0	1	1	77

first part  
of the count  
cycle

second part  
of the count  
cycle

Table 1. The content of the PROM in figure 6.

If we take as an example divisor 239 (which selects the highest tone in an octave),  $A_0 \dots A_3$  are logic 0. When  $A_4$  is low, the output of the PROM is 119 (77<sub>HEX</sub>), and when it is high, the output of the PROM is 120 (78<sub>HEX</sub>). The sum of the two is not a totally symmetrical square wave, but the very small deviation does not really matter.

If you want to experiment, it is, of course, possible to vary the ratios by programming different divisors. The phase relation between the harmonic frequencies is then also different, and this will affect the timbre.

**The final step**

An extended version of the previous circuit is shown in figure 8. Here again, the main modification lies in the tone divider. The memory range of the PROM has been expanded greatly, which enables the use of digitally controlled pulse-width modulation. The total divide time remains as

before, but the divisors for the logic 1 and logic 0 periods are different. If we take as an example a divisor of 447, a duty factor of, near enough, 50 per cent will split this into 223 and 224. If, however, a duty factor of 5 per cent is wanted, the first part becomes 20 (as the logic 1 can last only one tenth as long as before), and the second 427. Once again, we have the problem of having to divide the second part into two (because the 40103 still cannot cope with numbers larger than 256). Therefore, a second bistable, FF<sub>2</sub>, has been added; its Q output is taken to input A<sub>5</sub> of PROM IC<sub>5</sub>. In this way, a further division of both the first and the second part of the count cycle is effected.

Figure 9 illustrates what happens when a duty factor of 5 per cent is wanted. The divisors are 10 (1a), 10 (1b), 214 (2a), and 213 (2b). What was said earlier on about the relation between the sum of the stored preset values and the actual divisor is true here also. That is, preset value plus 1 is divisor. As this happens here four times, we must add 4 to the sum of 447 to obtain

**10**

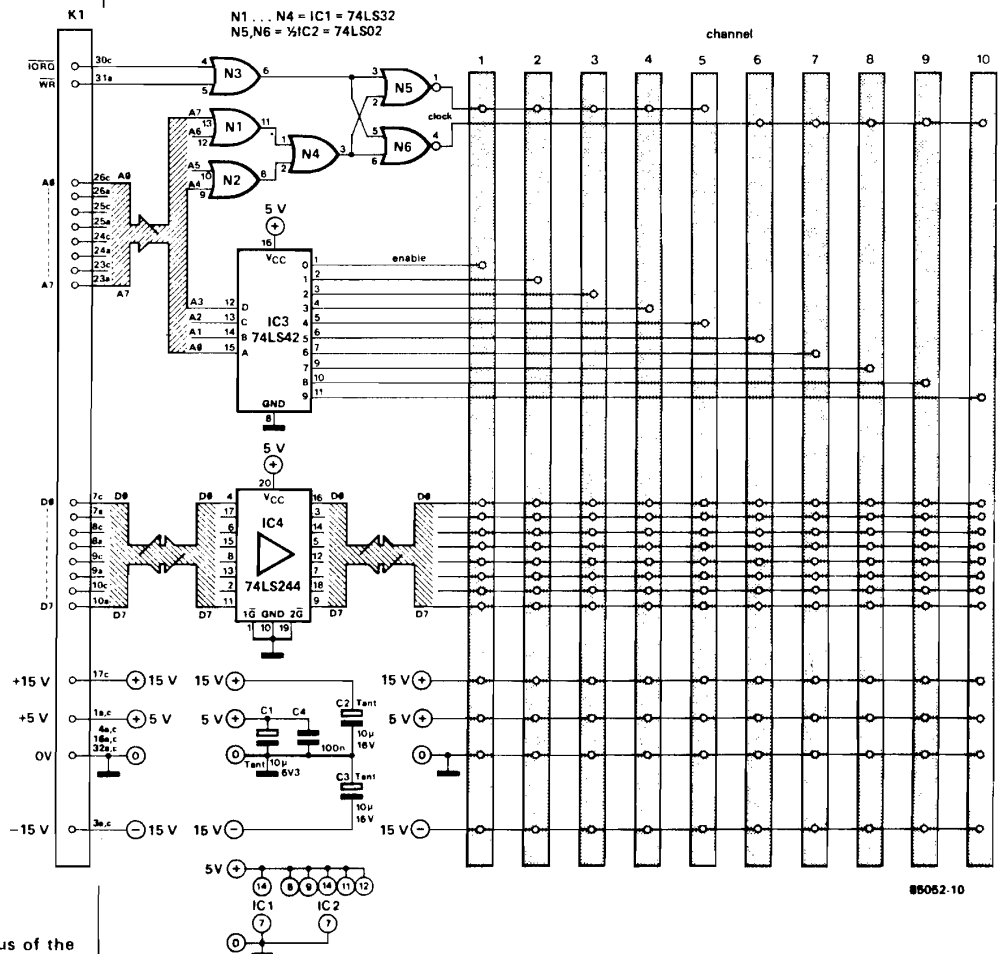


Figure 10. The bus of the polyphonic synthesizer can be connected to the DCOs in figure 2, 6 and 8 without any modification.

