# digisound SIGNAL PROCESSOR DEV-91

The DEV-91 dynamic signal processing board is an implementation of the circuitry contained within the CEM 3391 data sheet/application notes. The complete circuit diagram is shown in Figure 1, providing a VCF, a VCA, an ADSR and two output VCAs on a very compact PCB (60 x 84mm) which has been designed for maximum user flexibility.

The components should be positioned on the PCB according to the component overlay, Figure 2. All connections to and from the PCB (16 in all) are situated along one edge on a 0.1 inch pitch, suitable for male/female Molex connectors.

The power supply requirements for a single DEV-91 are +12V at 20mA, +5V at 3mA and -5V at 17mA.

Because of its great flexibility, this circuitry has many possible applications, such as:-

a) "Stand-alone" signal processing module.
With the addition of a number of potentiometer controls and jack sockets, the PCB may be configured for use as a "conventional" synthesiser module. All pots used should be 22k linear and wired as in Figure 3. The one exception to the standard wiring is the VCF cut-off frequency CV which requires a voltage range of +5V to -5V in order to provide adjustment over the VCF's entire range (Figure 4). If accurate keyboard tracking of cut-off frequency is required, a simple inverting summing op-amp may be used to derive a +1V/octave response, with simultaneous control via a potentiometer (Figure 5). In this format, an open collector TTL buffer (i.e. 1/6 7407) is recommended in order to preserve the switchable AR/ADSR to VCA characteristics. With the addition of a further resistor/zener diode network, the module may be gated from either +5V or +15V gate voltages (Figure 6).

The signal input resistor (R6) has been chosen to optimise on a 10V peak-to-peak input (decoupled by C3). For smaller signal inputs, this resistor value should be reduced to present an 85mV peak-to-peak signal to pin 14 of the CEM 3391.

b) Digital/computer-generated signal processor.
The circuitry of the DEV-91 is particularly suitable for microprocessor-based waveform processing, and with the addition of a DAC and multiplexing circuitry it can form an integrated part of a digitally based music production system. As the control inputs are all high impedance 0-4.5V inputs, a simple hold capacitor and multiplexer IC (e.g. 4051) are all that is required for interfacing to a DAC in order to achieve microprocessor control. This combination of digital waveform generation with computer controlled analogue processing can be seen in many existing synthesiser systems.

c) Multiple boards in a polyphonic system.
Use of strip-board or any motherboard bussing system allows simultaneous control of a number of signal processing boards from one control panel. The DEV-91 PCB is ideally suited for this type of application as all the "individual" (voice exclusive) inputs are at one end of the edge connector while the "common" connections (i.e. control inputs, mode switching and PSU rails) form the remainder. In this way, a motherboard for a 6 voice system could contain a single 7407, with each of the 6 buffers within this package dealing exclusively with a single channel gate input (with the addition of

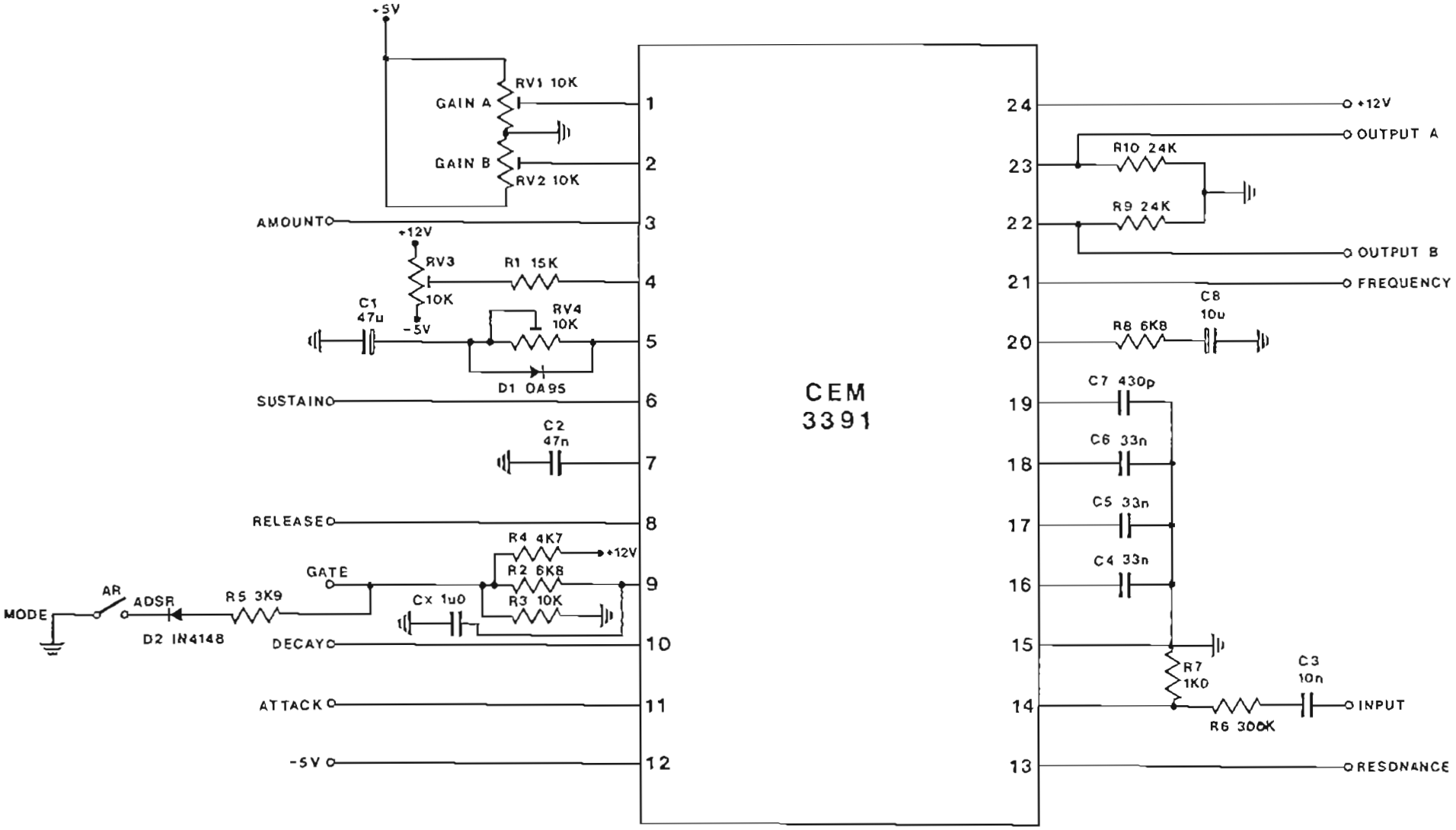


FIGURE 1. DEV-91 CIRCUIT DIAGRAM

resistors/zener diodes for +15V gating), and a dual op-amp could be used to mix the 6 pairs of outputs to a stereo output. In addition, the three power supply rails should be decoupled at least once and preferably twice, at either end of the motherboard. If individual VCF keyboard tracking is required, each frequency input must be accessed separately and each taken to an op-amp network as in Figure 5.

This type of configuration provides an extremely cost-effective signal processing arrangement, which with the addition of 6 or 12 oscillators (VCOs, VCDOs or DCOs) would form a high quality polysynth.

**COMPONENTS**

| RESISTORS, 5%, 1/4w carbon film | | CAPACITORS | |
|---|---|---|---|
| R1 | 15k | C1 | 47u PCB electrolytic |
| R2,8 | 6k8 | C2 | 47n polyester |
| R3 | 10k | C3 | 10n polyester |
| R4 | 4k7 | C4,5,6 | 33n polyester |
| R5 | 3k9 | C7 | 430p 1% polystyrene |
| R6 (see text) | 300k | C8 | 10u PCB electrolytic |
| R7 | 1k | CX | 1u PCB electrolytic |
| R9,10 | 24k | SEMICONDUCTORS | |
| | | IC1 | CEM 3391 |
| POTENTIOMETERS | | D1 | OA 95 |
| RV1,2,3,4 | 10k horizontal preset | D2 | 1N 4148 |

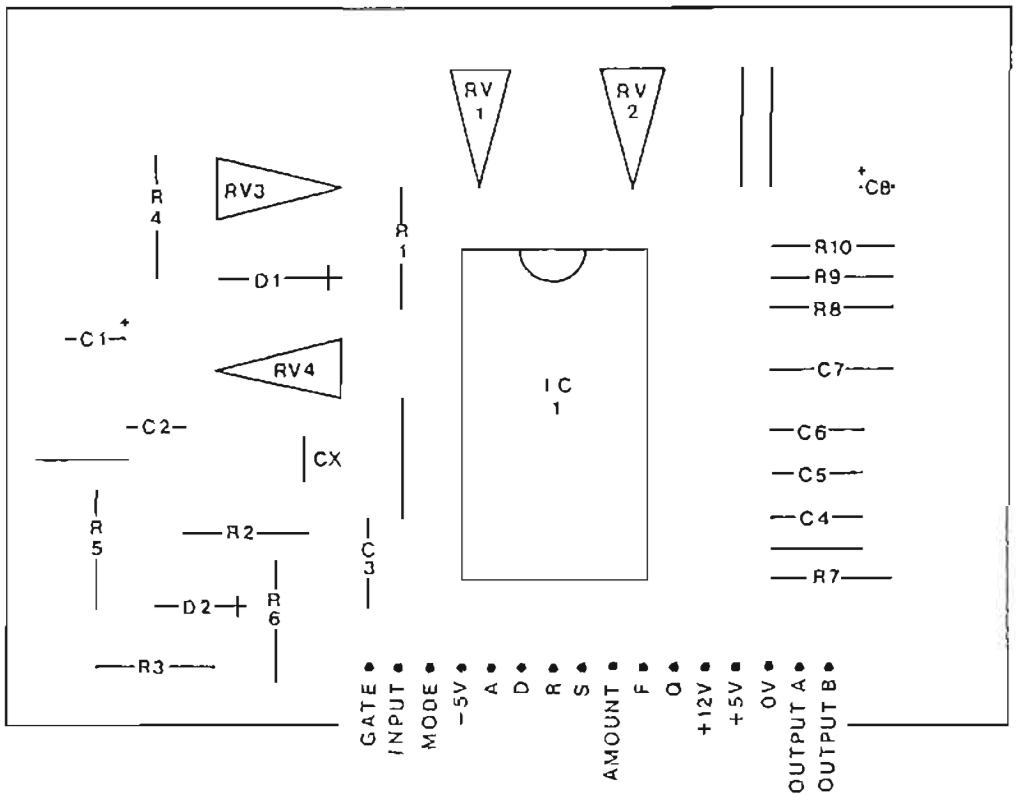


FIGURE 2. DEV-91 COMPONENT OVERLAY

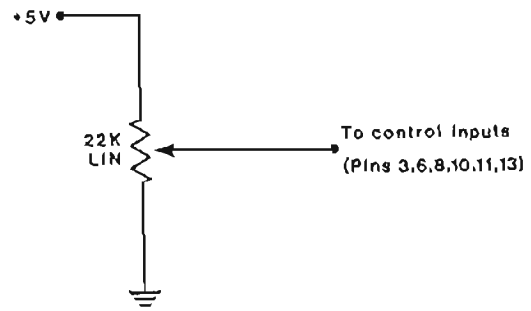


FIGURE 3.
Control pot
wiring

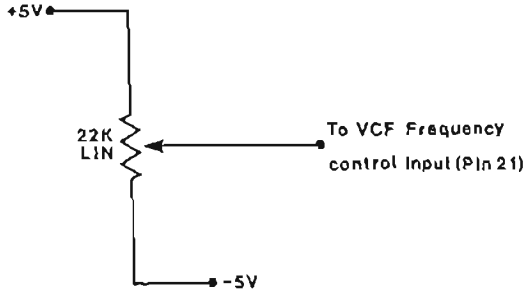


FIGURE 4.
VCF cut-off
frequency CV

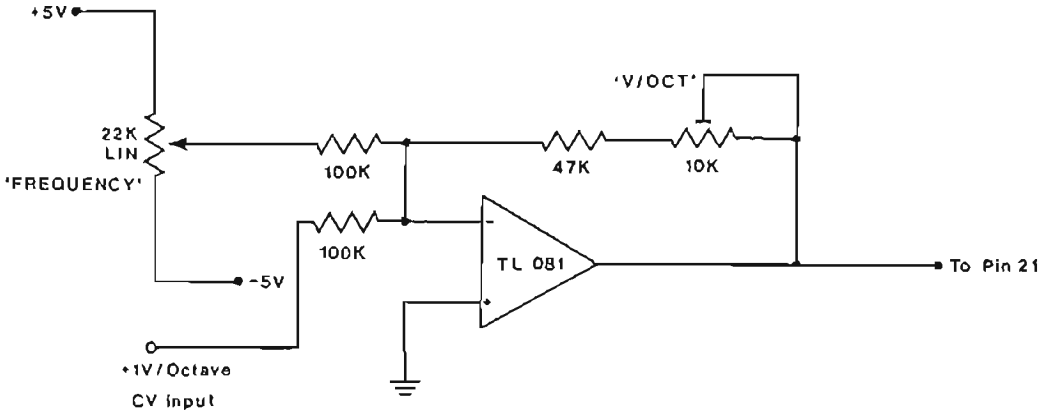


FIGURE 5.
VCF keyboard
tracking

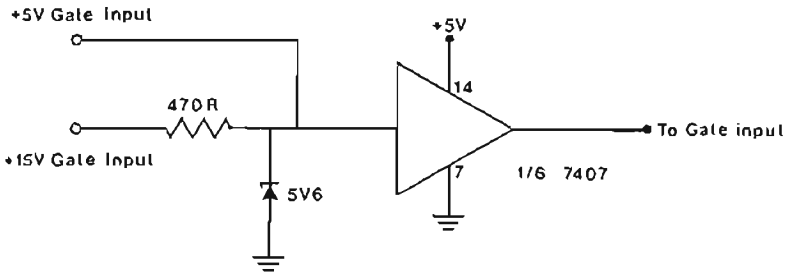


FIGURE 6.

# CEM 3391 Dynamic Signal Processor Application Hints

## Power Supplies

The maximum supply allowed across the chip (pin 12 to pin 24) is 25 volts. The positive supply may range from +11V to +16V while the negative supply may range from -4.5V to -12.5V. Thus +12V/-12V, +15V/-5V, and +12V/-5V would all be acceptable power supplies. For lowest warm-up and best performance, +12V/-5V supply is recommended.

## Envelope Amount VCA

The envelope amount VCA is a special design which allows either AC or DC coupling of the envelope into the VCF frequency control circuit. AC coupling with a 2-3 second time constant allows only fast changing portions of the envelope into the VCF while greatly attenuating or blocking the slower falling portions of the envelope; AC coupling is accomplished simply with a capacitor (47uF) connected to pin 5.

DC coupling, on the other hand, allows all portions of the ADSR envelope into the filter control, regardless of the rates. DC coupling is accomplished by connecting a 470R resistor (some resistance is necessary) from pin 5 to ground.

Two methods may be used to trim the envelope amount VCA. For DC coupling, a variable resistor with a range of 10k is connected from pin 5 to ground. With the envelope gated and set at maximum sustain, the trimmer is adjusted for the desired amount of filter sweep at a given envelope amount control voltage (usually at maximum). For AC coupling, the same trimming resistor is placed in series with the capacitor. During the trimming procedure, the capacitor is momentarily shorted to ground and the resistor adjusted as with DC coupling. When using AC coupling, a germanium diode (OA 95) should be placed across the resistance as shown in Figure 1 to allow fast discharge of the capacitor.

The second method for trimming entails using an external Sample & Hold for the envelope amount control voltage. The output of this Sample & Hold is then fed to pin 3 via a variable attenuator with a range from 70% to 100%. If AC coupling is used, the capacitor at pin 5 is momentarily shorted to ground while the attenuator is adjusted to give the desired filter sweep when maximum control voltage is applied to the Sample & Hold.

## Chip Time and Frequency Adjustment

The envelope generator time constants and VCF initial frequency will vary +/-35% from unit to unit. Pin 5 has been provided to trim both simultaneously with a single trim. The resistor connected to pin 4 is calculated as follows:-

$$R(\text{Kohm}) = 4(V_{EE} - 1.5)$$

where $V_{EE}$ is the negative supply voltage. Trimming may be accomplished by adjusting either the VCF frequency or attack time constant to the nominal value; the parameter not trimmed will then be within +/-15% of its nominal and other devices.

If it is desired to have both frequency and time constants track to a much tighter value, first the envelope time constants are adjusted with pin 4 and then the initial VCF control voltage adjusted with software or with an external Sample & Hold which includes a way of adding a trim voltage.

## Envelope Gate

The ADSR gate pin (pin 9) is a three level, dual function pin. From 0 to +2.5V, the envelope is gated off (release); from +2.5V to +5.0V, the envelope is gated on (attack, decay/sustain); from +5.0V to +8.5V, the envelope is gated on and a voltage is fed to the final VCA which turns it on completely at +8.5V. This allows the very popular class of sounds to be produced where the filter ADSR is enveloping the sound while the VCA is controlled only with a simple organ-like AR envelope.

If only the normal mode is desired, then pin 9 is connected to a TTL or CMOS logic signal through a 4k8 resistor (the resistor is always required since this pin connects to the emitter of an NPN). Figure 2 shows the interfacing required to implement both modes, where a single logic pull-down or mechanical switch can switch between the two modes for all devices. The capacitor connected directly to pin 9 slows the rise and fall times of the voltage fed directly to the VCA to about 20mS to suppress the clicks which would otherwise result from a fast VCA gating.

## Final VCA

The maximum output current from each VCA output is determined by the resistor in series with the capacitor from pin 20, and is calculated as follows:-

$$I_o(\text{mA P-P}) = 1.5/R$$

Best results are achieved with maximum output currents around 200uA P-P, which results in a resistor value of 6k8. Since the output currents typically are converted to voltages with other external resistors, use of an external resistor at this pin ensures better gain matching between devices.

An external signal (such as noise) may be coupled directly to the VCA input using this pin. Instead of connecting the other end of the capacitor to ground, it may be connected to the external signal. Since the output impedance of the external signal source will affect the maximum gain of the VCA, it should be kept much smaller than 6k8.