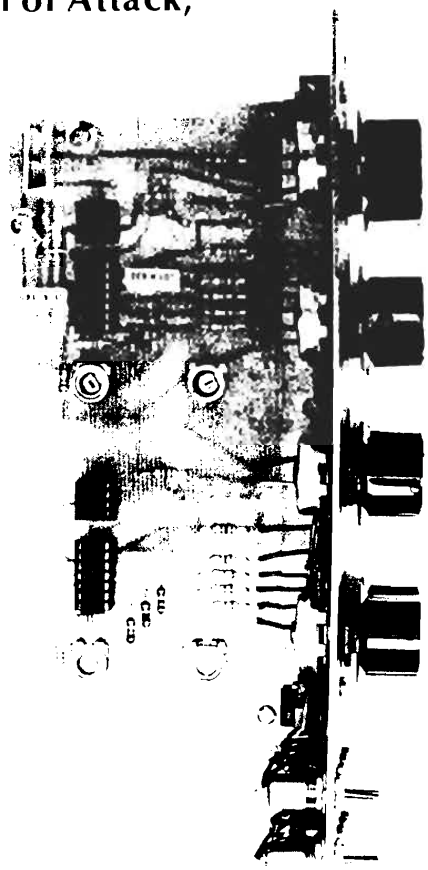
ENVELOPE SHAPER

Tamper with your time constants. This Project 80 design by R.C. Blakey gives full control of Attack, Decay, Sustain and Release.



The envelope generator is based on the SSM2050, a voltage controlled transient generator produced by Solid State Micro Technology. Using this IC all that is necessary to vary the time constants for the Attack (A), Initial Decay (D) and Final Decay or Release (R) is a voltage applied to the appropriate pin via a scaling resistor. A minimum range of 2 mS to 20 S is available for each of the three timing functions. The voltage response is exponential which means that the most useful time range utilises the highest proportion of the associated control potentiometer. The attack output is nominally 0 to 10 V and the Sustain level (S) is simply a voltage applied to Pin 12.

It has separate gate and trigger inputs whereby a combined gate and trigger pulse will initiate a full ADSR response, a trigger applied after the first one and while the gate pulse is still present will restart the attack response and a gate pulse on its own will generate an AD contour. When the gate pulse is released the final decay commences, as is usual with ADSR and AD envelope shapers.

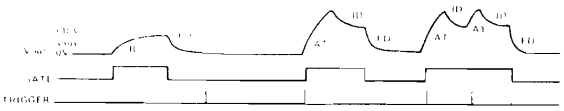


Fig.1. Wave forms associated with envelope processing.

The time constants may be trimmed so that any number of ADSR's can be adjusted to exactly the same scale. Also an adjustment to ensure that the sustain voltage accurately matches the peak attack voltage is provided. The output buffer in the SSM2040 is adequate for most practical purposes but to retain our 'plug in anything to anywhere' philosophy an external buffer has been added. Other features included are external initiation of the ADSR or AD contours, for example from a manual push button, as well as provision to use gate and trigger pulses derived from TTL logic.

Construction

The PCB is designed to take two envelope generators and as usual will fit either a panel or the TEKA ALBA A23C case. If the latter is used then there is only sufficient panel space to sensibly install a single envelope generator.

Construction is very straightforward and the only points to note are the single wire link and the opposed orientation of the SSM2050 and the 741 buffer.

An on-off switch, SW1, is connected across the inputs marked 'TRIGGER (CMOS)' and 'GATE (CMOS)' so that when only single pulses are available, eg, manual gating, then both the ADSR (SW1 closed) and AD (SW1 open) responses can be obtained. The manual gating can be added by connecting a push to make switch between the PCB connections marked 'OUTPUT FOR MANUAL GATE' and 'MANUAL GATE'. The push button may be panel mounted but the preferred approach is to take the former connection to a jack socket and to use an external hand, or foot, switch connected to two jack plugs. These jack plugs go to the Gate (G) input and the Manual input (from R11). The option and type of switch is left to the constructor.

Resistors R12, R13 and R14 are not part of the basic kit but are to be installed by constructors who are using TTL logic to derive gate and trigger pulses. Also in this case the switch, SW1, is connected across the PCB con-

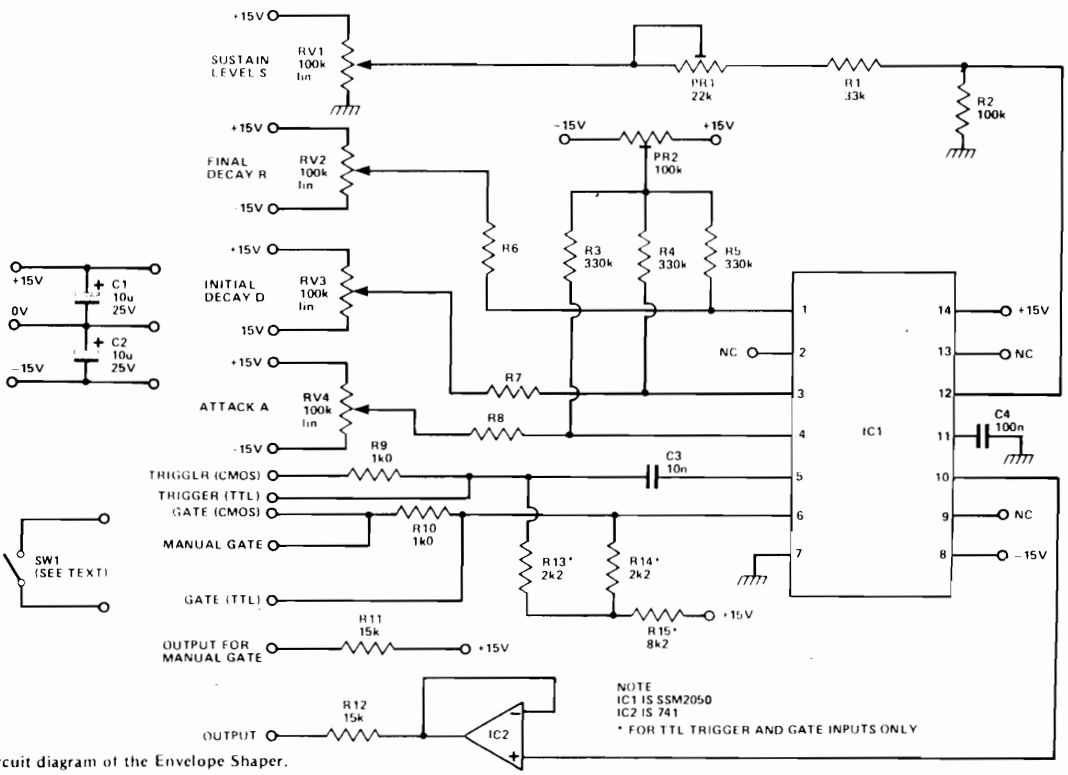


Fig.2. Circuit diagram of the Envelope Shaper.

HOW IT WORKS

The SSM2050 Voltage Controlled Transient Generator contains a voltage controlled resistor to generate the nominally exponential slopes and various logic devices to define the states. An attack flip-flop (AF/F) is set by the trigger pulse and reset by either NOT GATE or the attack comparator determining that the output has reached +10 V. Thus ATTACK = GATE and AF/F; INITIAL DECAY = GATE and NOT AF/F; FINAL DECAY = NOT GATE. Each state is characterised by a nominally exponential approach to a characteristic voltage; these being +13 V, sustain voltage and 0 V for attack, initial decay and final decay respectively.

The input stages of the SSM2050 logic inputs have a lateral PNP structure which protects them from excess voltages. Their sensitivity is 750 uA or 1V5 max., these being the minimum current and voltage required to trigger the SSM2050. For 5 V, 10 V and 15 V CMOS gate and trigger inputs these requirements are met using 1k, 10k and 15k resistors respectively to these inputs.

The attack, initial decay and final decay inputs have a nominal impedance of 8k1 and a time constant sensitivity of 18 mV/octave with a 100n timing capacitor (C4). An increasing positive voltage increases the time constant. Thus R6, 7 and 8, connected to +15 V via the rotary controls RV2, 3 and 4, will have nominal values of about 300k to achieve a five decade timing range from 2 mS to 20 S. The input impedance, however, varies by up to +25% between devices. Fortunately the impedance may be measured with a high input impedance ohm meter as the resistance between pins 1 and 7 and so the appropriate scaling resistor may be selected by multiplying this resistance by 100 and adding 10k. The nearest E24 resistor is chosen and more precise adjustment of timing is achieved by injecting a small offset voltage via PR2 and R3, 4 and 5. The attack voltage may vary between 10 and 11 volts and PR1, R1 and R2 provide a means of matching the maximum sustain voltage to the peak attack voltage. The sustain level can then be varied from 0 to 100% of attack voltage using RV1.

As an additional safeguard the output of the SSM2050 has been buffered by IC2 configured as a voltage follower.

nections marked 'TRIGGER(TTL)' and 'GATE(TTL)' to provide the same function as before. For manual gating with TTL a push to break switch should be connected between GATE(TTL) and 0V, since the gate and trigger pulses are held high by the additional resistors.

Setting Up And Calibration

Provide a means of manually gating the envelope generator as described in the previous section and the switch may be constructed from two strips of metal, if necessary. Connect the output to a voltmeter set to a DC range of 15V and turn Attack control (RV4) to about 3 o'clock position and all other external controls to zero. Put SW1 in the ADSR position (gate and trigger commoned), turn PR1 fully anti clockwise and PR2 about mid position. Apply power to the module, depress the manual button and keep held down while observing the voltmeter. The voltage should steadily rise and will probably take between 5 and 20 seconds to reach about 10V. Since the module is not calibrated the time taken may be outside of the range stated. The important point is that the voltage increases to a maximum of about 10V and then drops sharply to zero. If this response is observed then set Sustain control (RV1) to mid position and RV2, 3 and 4 to about the 3 o'clock position (a little less if the time to reach 10V was greater than 10 seconds in the previous step or a little more if the time was less than 5 seconds). Press button and hold down as before. The voltage should now rise to about 10V and then decay at the same rate to a voltage of approximately 5V and remain steady. On releasing the button there will be a final decay to about 0V. Finally, open switch SW1 to check

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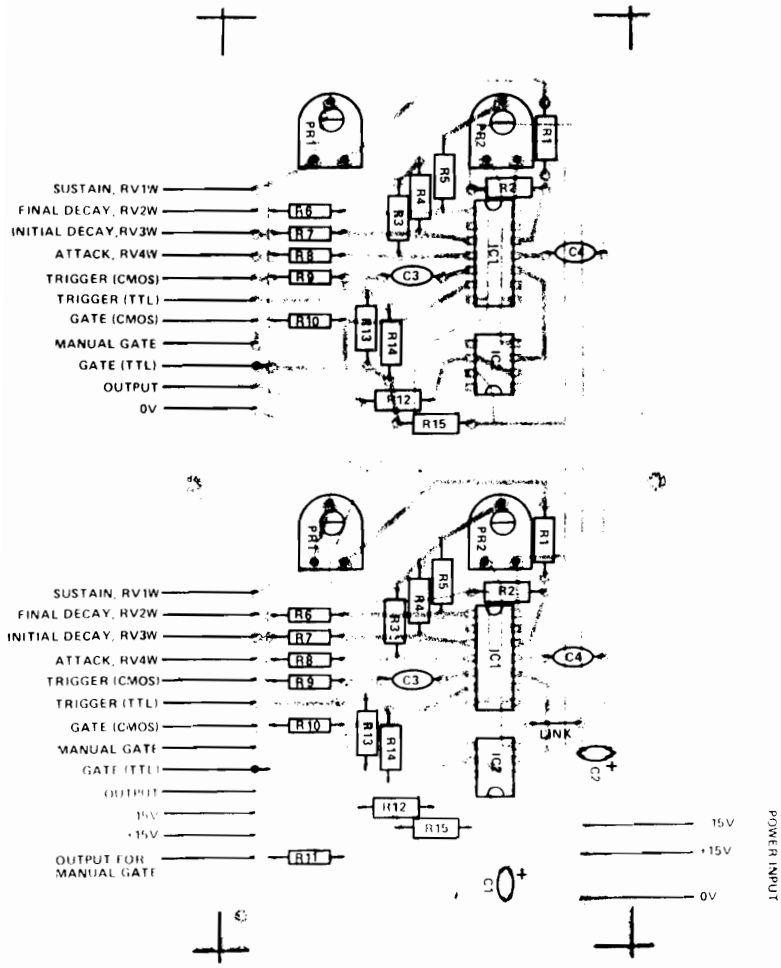


PARTS LIST

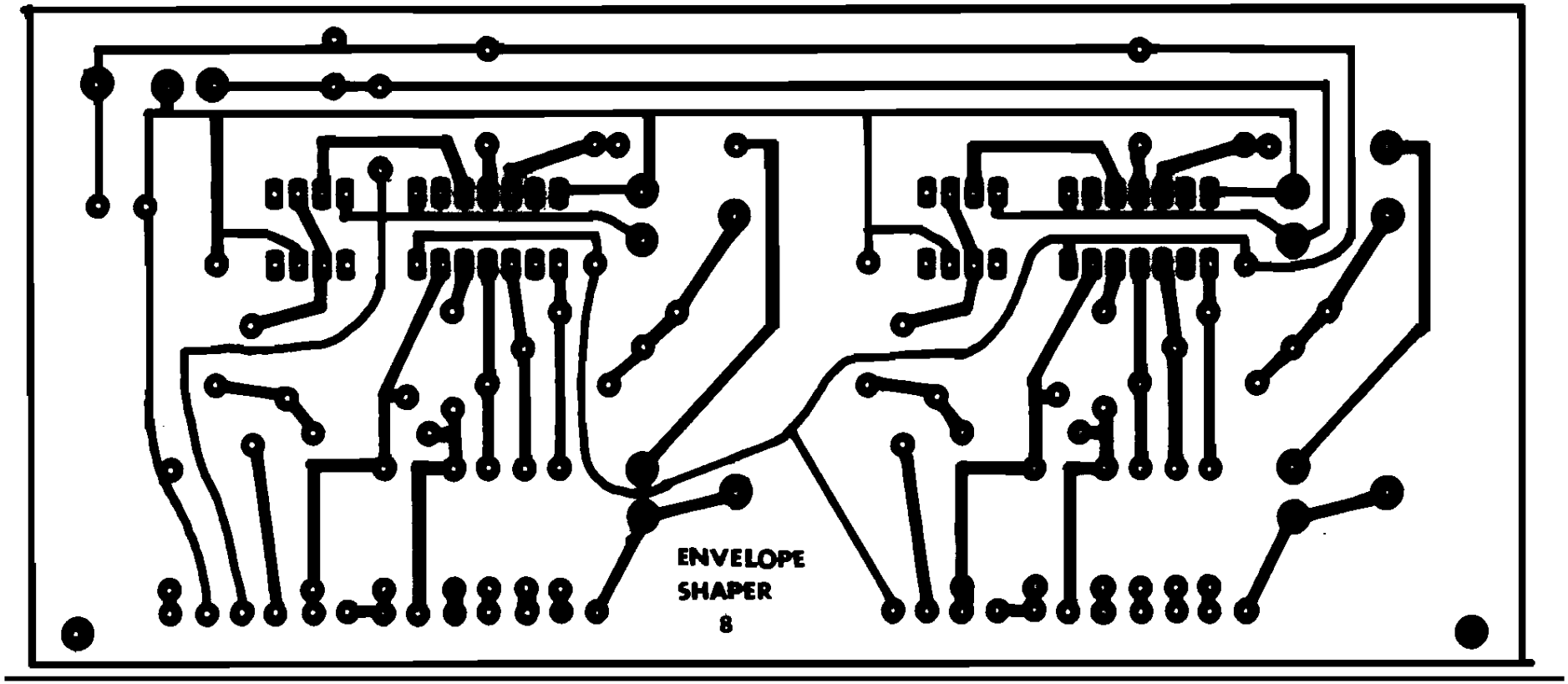
Resistors ¼W, 5% Carbon film	
R1	33k
R2	100k
R3,4,5	330k
R6,7,8	see text
R9,10,11	1k0
R11	15k
Potentiometers	
RV1,2,3,4	100k linear
PR1	22k carbon
PR2	100k carbon
Capacitors	
C1,2	10u 25V electrolytic
C3	10n polyester
C4	100n polyester
Semiconductors	
IC1	SSM2050
IC2	LM741CN, or equivalent
Miscellaneous	
SW1	Sub Min SPST (or SPDT) switch

Fig.3. Component overlay.

the AD response and repeat the last step. This time the voltage should rise to about 5V and maintain this value until the button is released which will initiate the decay to about zero. Note that in the AD mode the Initial Decay control (RV3) determines the attack time and the Sustain level controls the amplitude of the AD contour. The above demonstrates that all functions are operational.

The next step is to adjust the sustain voltage to match the peak attack voltage. Close SW1; set RV4 to about 3 o'clock, RV1 fully clockwise, RV2 and RV3 to the zero. Depress the manual button, observe the voltmeter and note whether there is a discernible drop in voltage after the attack has reached its peak. If so, turn PR1 clockwise and repeat the last step. Repeat until peak attack voltage and sustain level are matched. The adjustment to PR1 must be made in small increments so as to avoid having a higher sustain voltage than the attack voltage, otherwise malfunction of the SSM2050 can occur. It is therefore better to err on the safe side and wait until the envelope shaper is connected to the VCA at which time any mismatch between the two voltages can be checked by ear and a minor adjustment made to PR1 to correct it, if necessary.

The final step is to adjust the time constants and this calibration is only required for the Attack time control (RV4). The module should be in the ADSR mode (SW1 closed) and all other control pots set to zero. If an oscilloscope with a triggered sweep is available then the gate and the oscilloscope can be simultaneously triggered and PR2 adjusted to give an attack time of 2 mS when RV4 is at zero. An alternative method is to time the attack period, for example, by observing a voltmeter connected to the output and measuring the time between pressing the manual push button and the voltage dropping sharply. With the latter method adjust RV4 so that there is 10V0 at its wiper, trigger the module and adjust PR2 until the time taken is 9 S (slightly more than less). When this time is obtained turn RV4 to zero and check that a fast response time is obtained.


ENVELOPE
SHAPER
8